

BLP10H610

Broadband LDMOS driver transistor

Rev. 3 — 25 September 2014

Product data sheet

1. Product profile

1.1 General description

A 10 W plastic LDMOS power transistor for broadcast transmitter and ISM applications at frequencies from HF to 1400 MHz.

Table 1. Application performance

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
CW	27	50	10	26.7	46
	40	50	20	25	65
	60	50	19	24	65
	80	50	19	25	67
	88 to 108	50	16	25	62
	400 to 450	50	>14	>25.5	>62
	950 to 1225	50	>13	>16	>42
Pulsed RF [1]	860	50	10	22	60
	1190 to 1410	45	11	>14	-
DVB-T	860	50	1	>21	-

[1] t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1400 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

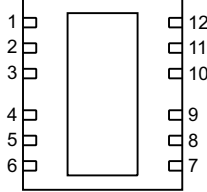
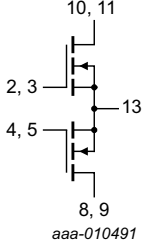
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 6, 7, 12	n.c.	 <p>Transparent top view</p>	 <p>aaa-010491</p>
2, 3	gate1		
4, 5	gate2		
8, 9	drain2		
10, 11	drain1		
13	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP10H610	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 × 6 × 0.85 mm	SOT1352-1

4. Limiting values

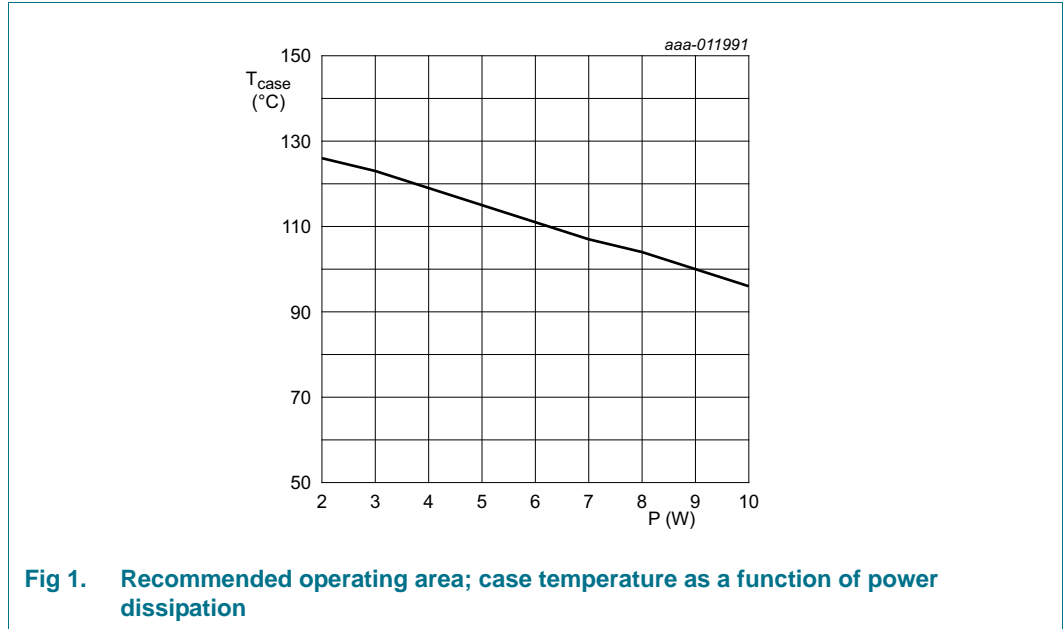
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	104	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C

5. Recommended operating conditions

See application note AN11520 for more details.



6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 10\text{ W}$ [1]	3.5	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions

7. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.12\text{ mA}$	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 12\text{ mA}$	1.25	1.75	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 60\text{ mA}$	1.4	1.8	2.15	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	1.88	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 420\text{ mA}$	-	2300	-	$\text{m}\Omega$

Table 7. AC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	0.13	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 0 V; f = 1 MHz	-	13.5	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	4.5	-	pF

Table 8. RF characteristics
Test signal: CW; f = 860 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 60 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _L = 10 W	19.3	22	25.7	dB
η _D	drain efficiency	P _L = 10 W	56.8	60	-	%

[1] The industrial test method is performed on special hardware to accommodate the requirements of production. The test results in this table are correlated to correspond with a performance in the application.

8. Test information

8.1 Ruggedness in class-AB operation

The BLP10H610 is capable of withstanding a load mismatch corresponding to VSWR = 35 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 60 mA; P_L = 10 W; f = 860 MHz.

8.2 Test circuit

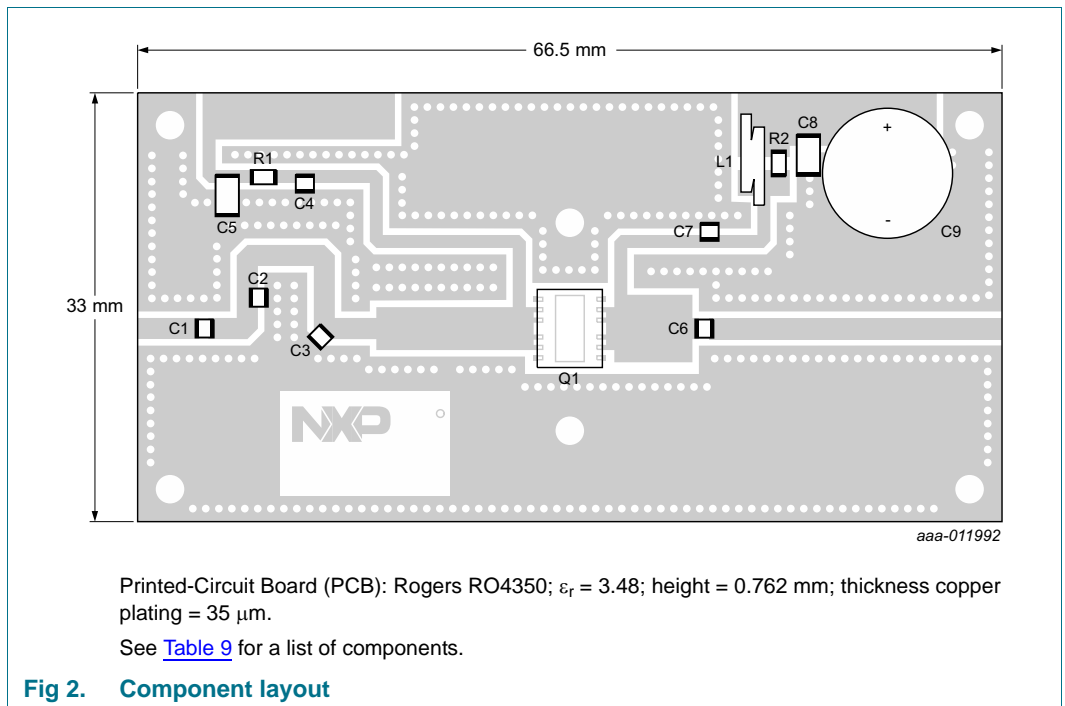
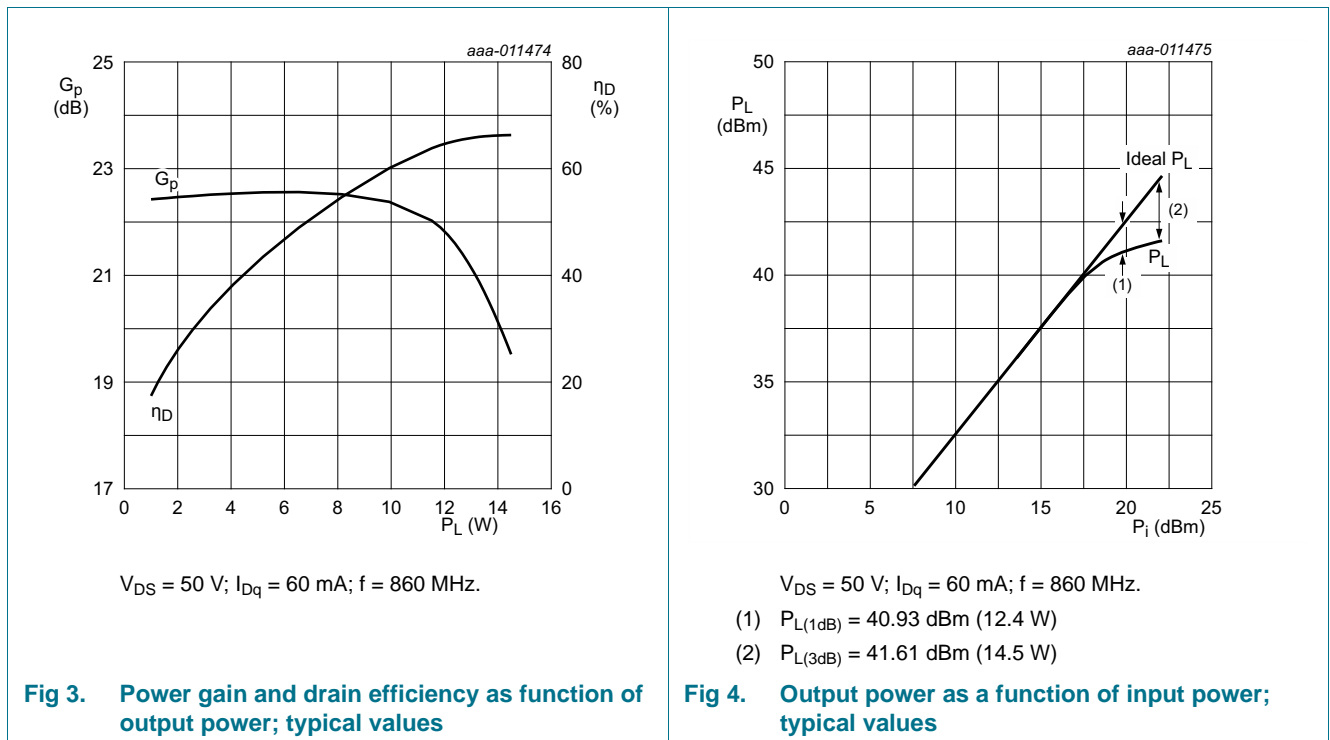


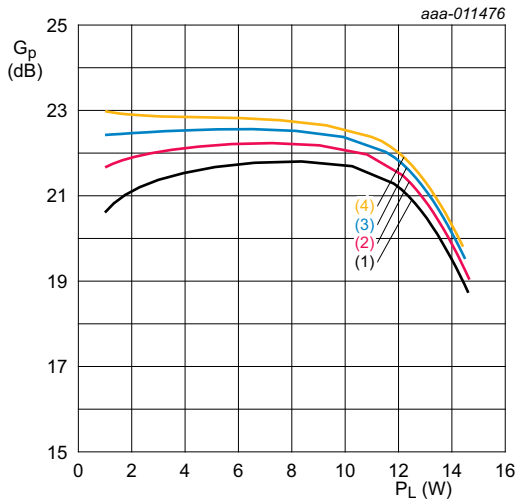
Table 9. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C4, C7	multilayer ceramic chip capacitor	100 pF	[1]
C2	multilayer ceramic chip capacitor	5.6 pF	[1]
C3	multilayer ceramic chip capacitor	3.9 pF	[1]
C5	multilayer ceramic chip capacitor	1 μ F, 25 V	Murata GRM31MR71E105KA01L
C6	multilayer ceramic chip capacitor	4.3 pF	[1]
C8	multilayer ceramic chip capacitor	1 μ F, 50 V	Murata GRM32RR71H105KA01L
C9	electrolytic capacitor	220 μ F, 63 V	
L1	wire inductor, 0.8 mm copper wire	2 turn, D = 3 mm	
R1	resistor	0 Ω	SMD 0805
R2	resistor	20 Ω	SMD 0805
Q1	transistor	-	BLP10H610

[1] American Technical Ceramics type 100A or capacitor of same quality.

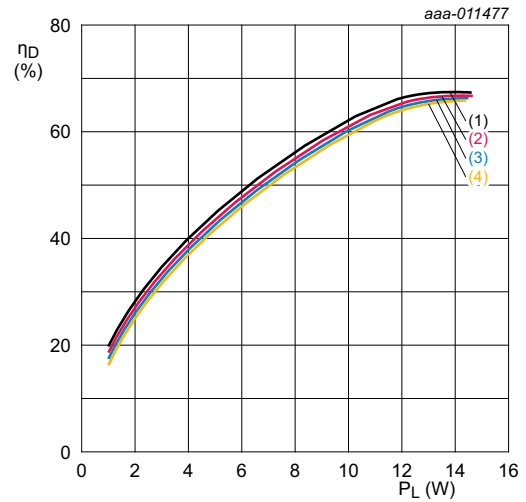
8.3 Graphical data





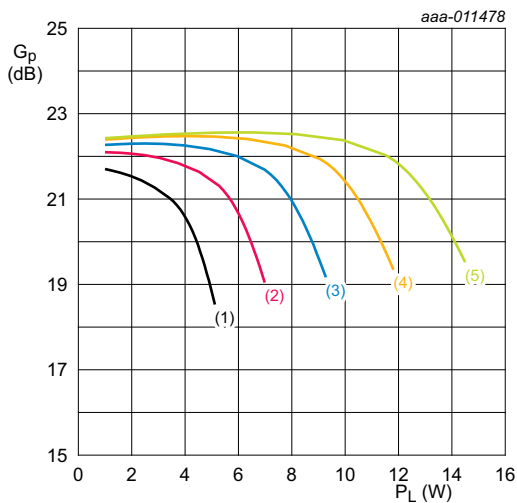
- $V_{DS} = 50\text{ V}$; $f = 860\text{ MHz}$.
- (1) $I_{Dq} = 20\text{ mA}$
 - (2) $I_{Dq} = 40\text{ mA}$
 - (3) $I_{Dq} = 60\text{ mA}$
 - (4) $I_{Dq} = 80\text{ mA}$

Fig 5. Power gain as a function of output power; typical values



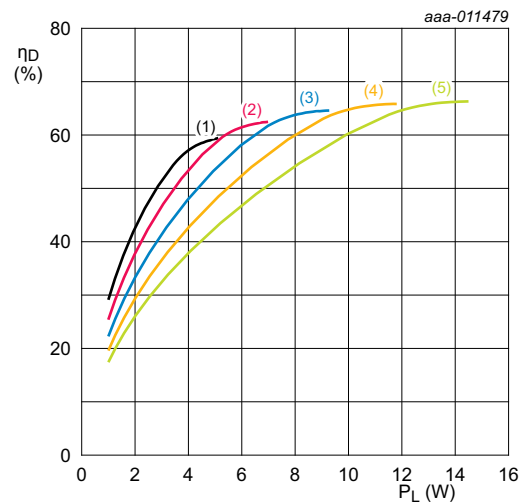
- $V_{DS} = 50\text{ V}$; $f = 860\text{ MHz}$.
- (1) $I_{Dq} = 20\text{ mA}$
 - (2) $I_{Dq} = 40\text{ mA}$
 - (3) $I_{Dq} = 60\text{ mA}$
 - (4) $I_{Dq} = 80\text{ mA}$

Fig 6. Drain efficiency as a function of output power; typical values



- $I_{Dq} = 60\text{ mA}$; $f = 860\text{ MHz}$.
- (1) $V_{DS} = 30\text{ V}$
 - (2) $V_{DS} = 35\text{ V}$
 - (3) $V_{DS} = 40\text{ V}$
 - (4) $V_{DS} = 45\text{ V}$
 - (5) $V_{DS} = 50\text{ V}$

Fig 7. Power gain as a function of output power; typical values



- $I_{Dq} = 60\text{ mA}$; $f = 860\text{ MHz}$.
- (1) $V_{DS} = 30\text{ V}$
 - (2) $V_{DS} = 35\text{ V}$
 - (3) $V_{DS} = 40\text{ V}$
 - (4) $V_{DS} = 45\text{ V}$
 - (5) $V_{DS} = 50\text{ V}$

Fig 8. Drain efficiency as a function of output power; typical values

9. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 5 x 6 x 0.85 mm

SOT1352-1

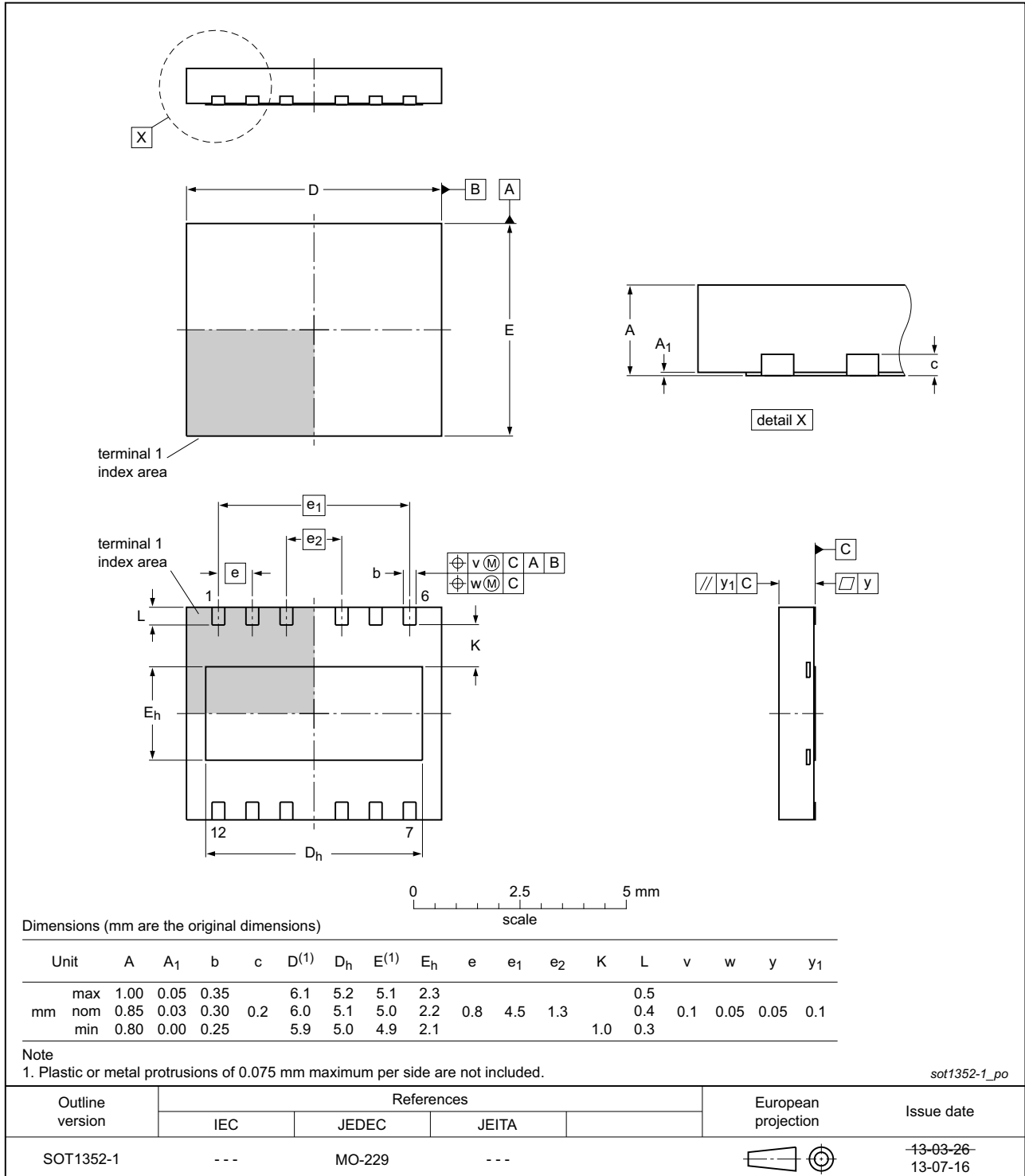


Fig 9. Package outline SOT1352-1 (HVSON12)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
HF	High Frequency
ISM	Industrial, Scientific and Medical
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H610 v.3	20140925	Product data sheet	-	BLP10H610 v.2
Modifications	<ul style="list-style-type: none"> Table 6 on page 3: several changes have been made Table 8 on page 4: several changes have been made 			
BLP10H610 v.2	20140422	Objective data sheet	-	BLP10H610 v.1
BLP10H610 v.1	20140120	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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